Attorney's Docket No.: 10559-075002/P7567C/Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Matthew J. Adiletta	Art Unit:	2183
Serial No.	: 10/615,500	Examiner:	Richard L. Ellis
Filed	: July 8, 2003	Assignee:	Intel Corporation
Title	: PARALLEL PROCESSOR ARCHITECTURE		

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant calls attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits of the Request for Continued Examination. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 22, 2006
Date of Deposit

Signature

Debbie Nast
Typed or Printed Name of Person Signing Certificate

Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any other charges or credits to deposit account 06-1050, referencing attorney docket 10559-075002.

Respectfully submitted,

Date: Feb. 22, 2006

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-075002	Application No. 10/615,500
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR 1.98(b))		Applicant Matthew J. Adiletta	
		Filing Date July 8, 2003	Group Art Unit 2183

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2004/0148382	07/29/04	Narad et al.			
	AB	2004/0109369	6/10/2004	Wolrich et al.			
	AC	2004/0098496	5/20/2004	Wolrich et al.			
	AD	2004/0073728	4/15/2004	Wolrich et al.			
	AE	2004/0071152	4/15/2004	Wolrich et al.			
	AF	2004/0054880	3/18/2004	Bernstein et al.			
	AG	2004/0039895	2/26/2004	Wolrich et al.			
	AH	3,736,566	5/29/1973	Anderson et al.			
	AI	4,709,347	11/24/1987	Kirk, David L.			
	AJ	4,890,218	12/26/1989	Bram			
	AK	4,890,222	12/26/1989	Kirk, David L.			
	AL	5,404,464	4/4/1995	Bennett			
	AM	5,404,469	4/4/1995	Chung			
	AN	5,459,843	10/17/1995	Davis			
	AO	5,485,455	1/16/1996	Dobbins et al.			
	AP	5,515,296	5/7/1996	Agarwal, Rohit			
	AQ	5,581,729	12/3/1996	Nistala et al.			
	AR	5,630,130	5/13/1997	Perotto et al.			
	AS	5,754,764	05/19/1998	Davis, et al.			
	AT	5,768,528	6/16/1998	Stumm			
	AU	5,781,551	7/14/1998	Born			
	AV	5,809,237	9/15/1998	Watts et al.			
	AW	5,898,701	4/27/1999	Johnson, David L.			
	AX	5,928,736	7/27/1999	Muller et al.			
	AY	5,933,627	8/3/1999	Parady et al.			
	AZ	5,938,736	8/17/1999	Muller et al.			
	BA	6,032,190	2/29/2000	Bremer et al.			

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	BB	6,067,300	5/23/2000	Baumert et al.			
	BC	6,141,677	10/31/2000	Hanif et al.			
	BD	6,272,520	8/7/2001	Sharangpani et al.			
	BE	6,282,169	8/28/2001	Kiremidjian			
	BF	6,295,600	9/25/2001	Parady et al.			
	BG	6,311,261	10/30/2001	Chamdani et al.			
	BH	6,393,026	5/21/2002	Irwin			
	BI	6,424,659	7/23/2002	Viswanadham et al.			
	BJ	6,477,562	11/5/2002	Nemirovsky et al.			
	BK	6,484,224	11/19/2002	Robins et al.			
	BL	6,526,451	2/25/2003	Kasper et al.			
	BM	6,553,406	4/22/2003	Berger et al.			
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	BO	6,629,236	9/30/2003	Aipperspach et al.			
	BP	6,631,422	10/7/2003	Althaus et al.			
	BQ	6,675,190	1/6/2004	Schabernack et al.			
	BR	6,678,746	1/13/2004	Russell et al.			
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	BT	6,826,615	11/30/04	Barall et al.			
	BU	6,876,561	4/5/2005	Wolrich et al.			
	BV	6,895,457	5/17/2005	Wolrich et al.			
	BW	6,925,637	8/2/2005	Thomas et al.			
	BX	6,952,824	10/4/2005	Hooper et al.			
	BY	6,976,095	12/13/2005	Wolrich et al.			
	BZ	6,983,350	1/3/2006	Adiletta et al.			

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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	CA	WO 01/16718	3/8/2001	WIPO				
	CB	WO 03/030461	4/10/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	CC	Chandranmenon, G.P. et al., "Trading Packet Headers for Packet Processing," IEEE/ACM Transactions on Networking 4(2): 141-152 (April 1996)
	CD	Dictionary of Computer Words: An A to Z Guide to Today's Computers, Revised Edition, Houghton Mifflin Company: Boston, Massachusetts, pp. 220, (1995)
	CE	Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller, Hardware Reference Manual, Digital Equipment Corporation, pages i-x, 1-1 through 1-5, 2-1 throught 2-12, 3-1 through 3-38, 4-31 through 5-2, 6-1 through 6-24, (March 1998)
	CF	News.Com, August 26, 1999. "Enterprise Hardware, Intel Expected to Unveil New Networking Chip," http://new.com.com/Intel+expected+to+unveil+new+networking+chip/2100-1001_3-230315.html (accessed on 08/23/05), pages 1-5

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